REMARKS

I.   Summary of Office Action

Claims 1-24 were pending in the above-identified patent application. Claims 11-24 have been withdrawn as being directed to an unelected invention.

Claims 1-10 were rejected under 35 U.S.C. § 102(b) as being anticipated by Owen et al. U.S. Patent No. 4,876,660 (hereinafter "Owen").

II.   Applicants' Reply to the § 102 Rejection

The Office Action rejected claims 1-10 as being anticipated by Owen. Owen refers to a fixed-point multiplier-accumulator architecture. *See* Owen, Abstract. Owen's FIG. 6A shows a functional block diagram of an emmitter-coupled logic (ECL) multiplier-accumulator. *See* Owen col. 7, 47-61; col. 9, ll. 19-61; and FIG. 6A.

Applicants claimed invention is generally directed to methods for initializing or zeroing an accumulator value with minimal latency. As recited by applicants' independent claim 1, a first pair of input signals and a second pair of input signals are routed to circuitry that is concentrated in a particular area of a programmable logic resource. For example, the input signals may be routed to one or more multiplier-accumulator blocks. A multiply operation is applied to the second pair of input signals using the circuitry. A feedback output, which is initially set to zero, is applied to the circuitry. Each signal of the first pair of input signal is concatenated with the feedback output in a first clock cycle. An accumulate operation is then applied to a result of the multiply operation and a result of the concatenating

in the same first clock cycle. A result of the accumulate
operation is then stored for use as an initialized or
zeroed accumulator value.

As recited by applicants' independent claim 8, a
pair of input signals is routed to circuitry that is
concentrated in a particular area of a programmable logic
resource. A multiply operation is applied to the pair of
input signals using the circuitry. A register is cleared
in the circuitry based on at least one dedicated
configuration bit that is set. A feedback output, which is
initially set to zero, is applied to the circuitry. The
contents of the register is concatenated with the feedback
output in a first clock cycle. An accumulate operation is
then applied to a result of the multiply operation and a
result of the concatenating in the same first clock cycle.
A result of the accumulate operation is then stored for use
as an initialized or zeroed accumulator value.

A.   Owen Does Not Concatenate Each Signal of a Pair of Input Signal and a Feedback Output

Applicants' independent claim 1 recites that each
signal of the first pair of input signals and the feedback
output (which is initially set to zero) are concatenated
and then this concatenated value is applied to an
accumulate operation. The Office Action contends that this
claimed feature is met by MUX 32 of Owen's FIG. 6A. *See*
Office Action, page 3. Namely, the Office Action contends
that "XA and YA are concatenated to form 32-bit into mux
32." *Id.* A prior Office Action alleged that this same
concatenation could alternatively be shown by "adder
component 34 wherein the first concatenation of the first
pair of input signals is done by the first input port of

the mux 32 and the second concatenation of the first concatenation result with the initial '0' feedback value/result . . . is done by the adder from 32 bits input to 41 bits output." *See* January 11, 2008 Office Action, page 7. Applicants respectfully disagree and submit that neither adder 34 nor MUX 32 of Owen's FIG. 6A shows applicants' claimed concatenating.

MUX 32 in Owen's FIG. 6A does not concatenate any feedback output which is initially set to zero, as recited by independent claim 1. Rather, what the Office Action contends is the feedback output (i.e., a zero input to MUX 56) is fed into MUX 56, and the output of MUX 56 is connected to adder 34. At no point does FIG. 6A show a pair of input signals and a feedback output (which is initially set to zero) concatenated and then applied to an accumulate operation.

Similarly, applicants' independent claim 8 also recites that the contents of a register are concatenated with the feedback output (which is initially set to zero). As with independent claim 1, the Office Action contends that the feedback output is a zero input to MUX 56. This feedback output, however, is not concatenated with any register value and then applied to an accumulate operation. Rather, registers 14 and 16 are concatenated to form a 32-bit input to MUX 32. *See* Owen, FIG. 6A

Adder 34 also does not concatenate a pair of input signals and a feedback output (which is initially set to zero). Rather, adder 34 adds the output of MUX 32 and the output of MUX 56. As stated in Owen:

> In a 16 X 16 multiplier, this result includes 32 parallel bits consisting of sixteen least significant bits and sixteen most significant

bits, each ordered from least to most significant
bits. The result is input to a first or product
input port 36 of an adder 34. A multiplexer
function 32 selects, as the result to be input to
the adder, either the product of multiplication,
the result of concatenation, or zeroes. The
adder has a second, accumulator contents input
port 38. The result, and another binary number
input via port 38 are added by adder 34.
See Owen, col. 8, ll. 10-20.

As such, it is clear that although adder 34 may
output 41 bits, adder 34 itself performs no concatenation.
The only concatenation performed prior to adder 34 occurs
just before MUX 32, where the 16-bit X operand may be
concatenated with the 16-bit Y operand. MUX 32 may then
output this concatenation, zeros, or the product of the
multiplication from multiplier 30. *See* Owen, FIG. 6A. At
no time does FIG. 6A show a pair of input signals and a
feedback output (which is initially set to zero)
concatenated and then applied to an accumulate operation.

B.   Owen Does Not Concatenate and Apply an
     Accumulate Operation on a Result of the
     Concatenating and a Result of a
     Multiply Operation in the Same Clock Cycle

Applicants previously amended both independent
claims 1 and 8 to recite that the concatenating described
above and the application of an accumulate operation on a
result of a multiply operation with a result of the
concatenating were performed in the same clock cycle. This
is possible, for example, "using circuitry in the MAC block
that is typically not used during a multiply-and-accumulate
operation" (Specification, ¶ 0008). By utilizing this
circuitry, applicants' claimed invention allows for an
accumulator value to be initialized or zeroed with minimum

latency.

The Office Action states that in Owen's FIG. 6A, "the series of operations are operated in series/pipeline manner wherein all the operations are operated at the same time but on different set of data." Office Action, pages 5-6. The Office Action also alleges that "the concatenating is done on the input pair of signals wherein the accumulator is done on the output of multiplexer 32 and the feedback of previous result by multiplexer 56." Office Action, page 6.

However, as described above, applicants' claimed concatenating operates on each signal of a pair of input signals and a feedback output that is initially set to zero (claim 1) or the contents of a register and a feedback output that is initially set to zero (claim 8). Even if all the operations in Owen's FIG. 6A were performed in the same clock cycle, the result of Owen's concatenating would not be available for an accumulate operation with the result of any multiply operation in the same clock cycle. *See* Owen, FIG. 6A.

For at least the foregoing reasons, applicants submit that independent claims 1 and 8 are allowable over the prior art of record. Dependent claims 2-7, 9, and 10 are allowable for at least the same reasons. Applicants respectfully request, therefore, that the rejection of claims 1-10 under 35 U.S.C. § 102 be withdrawn.

III.   Conclusion

Applicants respectfully submit that this application, including claims 1-10, is now in condition for

allowance. Accordingly, prompt consideration and allowance of this application are respectfully requested.

Respectfully submitted,

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